R22 Regulation *Subject code: 4P8DH*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VIII Semester Regular Examinations, May 2026

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(ECE)

Maximum Marks: 60 Date:06.05.2026 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X1M=10 Marks)		Marks	CO	BTL
1.a)	Define signal-to-quantization-noise ratio (SQNR).	1M	1	1
b)	What is DFT?	1M	1	2
c)	What is cache Memory?	1M	2	1
d)	What is throughput?	1M	2	1
e)	Name one real-time application of DSP.	1M	3	1
f)	What is dual-access RAM?	1M	3	1
g)	Explain Timer peripheral.	1M	4	1
h)	Name one peripheral in Blackfin processor.	1M	4	1
i)	What is memory access time?	1M	5	1
j)	List out various data transfer methods.	1M	5	1

Part-B

Answer All the following questions. (5X10M=50Marks)		Marks	CO	BTL
2	a) Explain A/D Conversion errors and DSP Computational errors.	5M	1	2
	b) What is Compensating filter, explain with suitable examples.	5M	1	2
	OR			
3	Draw the block diagram of a DSP System and explain in detail the function of each block.	10M	1	2
4	a) List the DSP Computational Building Blocks, explain any two blocks.	5M	2	2
	b) Discuss about the speed issues in DSP processors.	5M	2	2
	OR			
5	Discuss in brief about the data addressing capabilities of programmable DSP devices with examples.	10M	2	3
6	a) Explain memory management and memory space in TMS320C54XX DSP processors.	5M	3	2
	b) What are the different on-chip peripherals in TMS320C54XX processor? Explain.	5M	3	2
	OR			

7	Define addressing mode, explain any four Data Addressing modes of TMS320C54XX Processors.	10M	3	3
8	Explain the Micro Signal Architecture for DSP processors with a diagram.	10M	4	2
	OR			
9	a) With the help of block diagram explain functionality of ADSP-2181 high performance Processor.	5M	4	3
	b) Explain Address Arithmetic Unit and Control Unit with a diagram.	5M	4	3
10	Explain interfacing of memory to programmable DSP devices.	10M	5	2
	OR			
11	Draw the diagram of DMA. Explain its importance in increasing speed of a DSP processor.	10M	5	3